W-band InP/InGaAs/InP DHBT MMIC Power Amplifiers

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Abstract — **We report W-band MMIC class A power amplifiers in InP/InGaAs/InP DHBT transferred-substrate technology. A cascode amplifier with 64 μm² emitter area exhibits a peak small-signal gain of 10 dB at 90GHz and an output power of 9.5 dBm under 1 dB gain compression. An 8.5-dB-gain common-base amplifier with an emitter area of 128 μm² delivers 14 dBm output power at 85 GHz under 1 dB gain compression and 16.2 dBm (42 mW) saturated output power with an associated 4.6 dB gain. To our knowledge, this is highest reported output power for a W-band HBT power amplifier.**

I. Introduction

Deep submicron InP-based HEMTs have established record power levels for W-band solid-state power amplifiers [1], substantially exceeding the power levels attained by HBTs. Scaling of InP-based HBTs has resulted in devices with high cutoff frequencies, enabling high-gain amplifiers in W-band [2,3] and at 175 GHz [4]. Unfortunately, these wideband HBTs have low breakdown voltage and hence low output power. We had recently reported [5] 0.5 um InP DHBTs with combined wide bandwidth (425 GHz f_{max}) and high breakdown voltage ($V_{BR,CEO}$ > 8 Volts). Here we report W-band InP DHBT amplifiers in this technology that deliver 42 mW (16.2dBm) saturated output power, substantially larger than previously reported for HBTs in W-band.

II. Device Technology

The circuits were fabricated using a substrate transfer process [2,3,4]. DHBTs with InP collectors are employed for high breakdown voltages. The epitaxial layer structure is similar to that reported in [5] with a 400-Å-thick InGaAs base and a 3000-Å-thick InP collector and the wafer was grown by IQE Inc. InAlAs/InGaAs digital alloy grades are employed in both the emitter-base and base-collector junctions. In transferred-substrate HBTs, the device is inverted, and heat must flow from the semiconductor junction to the substrate through the emitter semiconductor. InP has ~15:1 higher thermal conductivity than InAlAs, and hence is employed as the DHBT emitter.

The transferred-substrate process substantially reduces the collector-base charging time $R_{bb}C_{cbi}$ and hence increases the HBT f_{max}. Power DHBTs are realized with a multiple-finger structure in the same process. Finger spacing must be adequate for minimal finger-finger thermal coupling, emitter ballast resistances are provided to prevent thermal instability (current hogging) [6] at the intended V_{CE} and J_c. The emitter fingers have 16 μm × 1 μm mask dimension with a corresponding 20 μm × 2 μm collector finger. Each emitter finger employs an 8 Ohm NiCr ballast resistor. In the circuits, the HBTs are biased to set the peak instantaneous current density at 1×10^5 A/cm². While the breakdown voltage of the common emitter power DHBT is greater than 8 volts at low current density, maximum operating voltage at high current density is determined by thermal instability, and is a function of the emitter ballast resistance. Both 4-finger and 8-finger devices (with emitter areas of 64 μm² and 128 μm² respectively) exhibit f_{max} above 330 GHz.

The process provides a micro strip wiring environment on a thin 5 μm BCB polymer dielectric with ε_{eff} =2.7. Smaller circuit capacitances use the polymer dielectric, while larger circuit capacitances are realized using MIM structures with 0.4 μm thickness SiN dielectric. Resistors are fabricated using thin-film NiCr that has a sheet resistance of 40 Ohms/square.

III. Circuit Design

Figures 1 and 3 show the die photographs of the cascode and common-base amplifiers, while figures 2 and 4 show the circuit schematics. Each amplifier consumes a die area of 0.5mm × 0.4mm.

The common-base design (Fig.1 and Fig.2) uses 2 parallel 4-finger power DHBT cells, forming a composite 8-finger device with 128 μm² emitter junction area. Because of the very low impedance, the input of the two paralleled 4-finger common-base devices are interconnected with inductive microstrip lines and then matched to 50 Ω with a shunt capacitance. The device is biased at 78 mA (0.6×10^5 A/cm²) and V_{CE} =3.6 Volts. The output is tuned with two cascaded Π-sections. At

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the design frequency, the output tuning network loads the HBT in the optimum admittance for saturated output power as $Y_{L,opt} = G_L + jB_L$, where the load susceptance $B_L = -\omega C_{cb}$ compensates for the HBT output capacitance and $G_L = I_{c,\max}/(V_{CE\max} - V_{CE,sat})$ is the optimum load conductance. With design values of $V_{CE,\max}$=6.1 V, $V_{CE,sat}$ = 1.1 V, and $I_{C,\max}$=128 mA, G_L is $1/40\,\Omega^{-1}$ and the expected saturated output power is $P_{sat} = I_{C,\max}(V_{CE,\max} - V_{CE,sat})/8$=80mW.

In the cascode design (Fig.3 and Fig.4), both the common-emitter and common-base HBTs are 4-finger (64 μm^2) devices. The output common-base device is biased at 40 mA ($0.63x10^5$A/cm^2) and V_{CE}=3.5 Volts, hence the expected saturated output power is 40 mW. The input is matched for maximum gain using a T-section tuning network, while the output tuning network is a shunt inductive stub and a quarter-wave transformer.

The tuning networks uses capacitors with both SiN and BCB dielectrics. The SiN capacitors have much larger capacitance per unit die area, but have substantially larger processing variability due to variations in the thickness of the deposited dielectric film. Parallel combinations of the two, with capacitances appropriately partitioned between the SiN and BCB elements, result in a compact IC layout with reduced processing variability.

IV. Testing

Amplifier small-signal gains and return losses were measured on-wafer using GGB wafer probes and a W-band Agilent 8510 network analyzer calibrated with a commercial LRM substrate. For power measurements, the amplifiers were driven by a W-band frequency multiplier and power amplifier, and the output power measured directly with a power meter without additional off-wafer load impedance tuning. The data is corrected for the measured attenuation of wave guides and wafer probes.

IV. Results

Figure 5 shows the small-signal characteristics of the common-base power amplifier, while gain compression and saturation power data are shown in figure 6. The insertion gain is 8.5 dB while the 1 dB compression output power is 14 dBm at 85 GHz. The saturated output power is 16.2 dBm (42 mW) with a corresponding gain of 4.6 dB.

The cascode amplifier exhibits an insertion gain (S_{21}) of 10 dB when biased for peak gain and 8.5 dB when biased for maximum saturated power at 90 GHz, with the input and output return losses greater than 10dB. Fig. 7 shows the measured small-signal characteristics. Fig. 8 shows the gain and saturated power characteristics at 90 GHz. The amplifier has an output power of 9.5 dBm under 1 dB gain compression and the saturated output power is greater than 12 dBm.

IV. Conclusions

The InP/InGaAs/InP transferred-substrate DHBT MMIC technology provides high breakdown voltages whose bandwidth is sufficient for W-band applications. Output power can be directly increased by increasing the transistor emitter junction areas and by power-combining several stages. With attained DHBT cutoff frequencies of 330-425 GHz, G-band (140-220 GHz) power amplifiers are also feasible.

Acknowledgement

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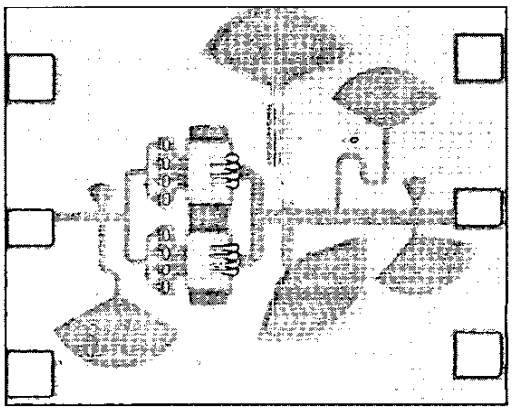

Figure 1: Common-base amplifier die photograph.

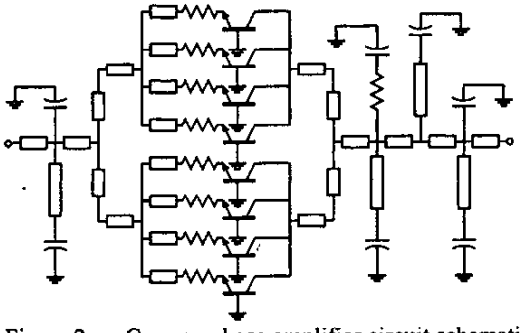

Figure 2: Common-base amplifier circuit schematic.

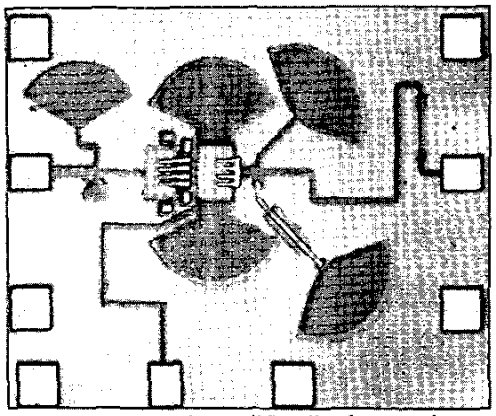

Figure 3: Cascode amplifier die photograph

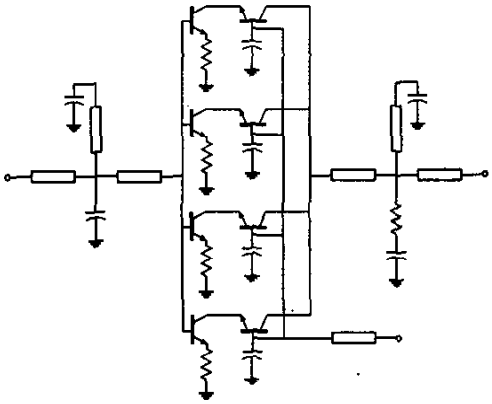

Figure 4: Cascode amplifier circuit schematic

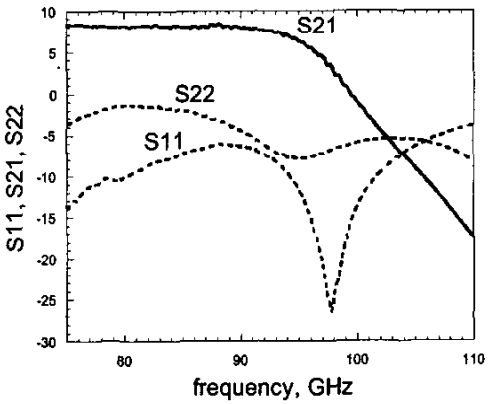

Figure 5: Small-signal parameters of the common-base power amplifier

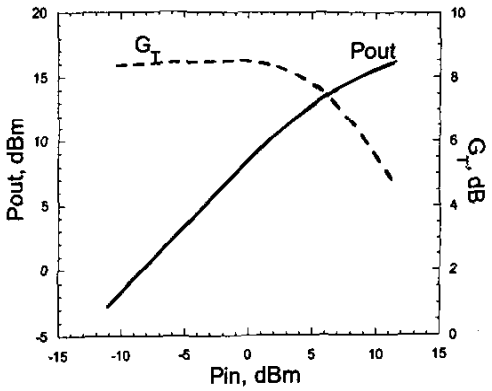

Figure 6: Power saturation characteristics of the common-base power amplifier

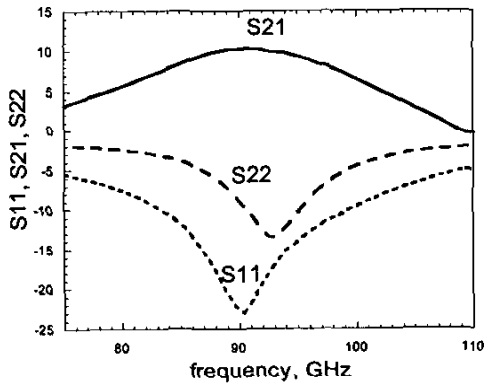

Figure 7: S-parameters of the cascode power amplifier when biased for peak small-signal gain

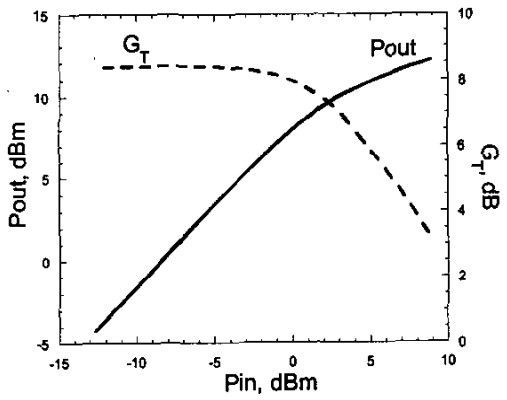

Figure 8: Power saturation characteristics of the cascode power amplifier

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